WHAT IS CLAIMED IS:

1. A semiconductor memory device comprising:

a semiconductor substrate;

a tunnel insulating film formed on said semiconductor substrate;

an Al_2O_3 film formed on said tunnel insulating film;

a pair of charge storage layers sandwiching said Al_2O_3 film therebetween in plain view formed on said tunnel insulating film;

an insulating film formed on said Al_2O_3 film and said pair of charge storage layers;

a gate electrode formed on said insulating film; and

a source region and a drain region formed as a pair sandwiching said gate electrode in plain view formed on a surface of said semiconductor substrate.

2. The semiconductor memory device according to claim 1, further comprising a sidewall insulating film formed over a side surface of said gate electrode, said insulating film, and said pair of charge storage layers.

3. A semiconductor memory device having a pair of charge storage layers in each memory cell thereof and being capable of storing four values, comprising an Al_2O_3 film insulating said pair of charge storage layers with each other.

4. The semiconductor memory device according to claim 1, wherein

said charge storage layers are composed of a polycrystalline silicon.

5. The semiconductor memory device according to claim 3, wherein

said charge storage layers are composed of a polycrystalline silicon.

6. The semiconductor memory device according to claim 1, wherein

said tunnel insulating film has a thickness of 3 nm to 9 nm.

7. The semiconductor memory device according to claim 3, wherein

a tunnel insulating film has a thickness of 3 nm to 9 nm.

8. The semiconductor memory device according to claim 1, wherein

said Al_2O_3 film and said pair of charge storage layers have a thickness of 5 nm to 15 nm.

9. The semiconductor memory device according to claim 3, wherein

said Al_2O_3 film and said pair of charge storage layers have a thickness of 5 nm to 15 nm.

10. A manufacturing method of a semiconductor memory device comprising the steps of:

forming a tunnel insulating film on a semiconductor substrate;

forming sequentially an Al_2O_3 film, an insulating film, and a material film of a gate electrode on the tunnel insulating film;

forming a gate electrode by processing the material film of the gate electrode, the insulating film, and the Al_2O_3 film into a planar shape of the gate electrode;

making a retreat of an outer edge of the Al_2O_3 film to be smaller than an outer edge of the gate electrode by performing isotropic etching to the Al_2O_3 film so as to form a pair of spaces under the insulating film;

forming charge storage layers respectively in the pair of spaces; and

forming a source region and a drain region sandwiching the gate electrode in plain view, as a pair, on a surface of the semiconductor substrate.

11. The manufacturing method of the semiconductor memory device according to claim 10, wherein

isotropic etching of the Al_2O_3 film is performed using a solution of sulfuric acid with hydrogen peroxide during the step of performing isotropic etching to the Al_2O_3 film.

12. The manufacturing method of the semiconductor memory device according to claim 10, wherein

a polycrystalline silicon film is formed as the charge storage layers.

13. The manufacturing method of the semiconductor memory device according to claim 10, wherein

said step of forming the charge storage layers comprises the steps of:

forming a polycrystalline silicon film all over surface; and

making the polycrystalline silicon film remain in the spaces and forming a sidewall composed of the polycrystalline silicon film over side surfaces of the gate electrode and the insulating film by performing anisotropic etching to the polycrystalline silicon film.

14. The manufacturing method of the semiconductor memory device according to claim 13, wherein

said step of forming the charge storage layers comprises a step of oxidizing the sidewall after the step of performing anisotropic etching to the polycrystalline silicon film.

15. The manufacturing method of the semiconductor memory device according to claim 10, wherein

said step of forming the charge storage layers comprises the steps of:

forming a polycrystalline silicon film all over surface; and

making the polycrystalline silicon film remain only in the spaces by performing anisotropic etching to the polycrystalline silicon film.

16. The manufacturing method of the semiconductor memory device according to claim 15, wherein

said step of forming the charge storage layers comprises the steps of:

forming an insulating film for a sidewall all over surface; and

forming a sidewall insulating film over side surfaces of the gate electrode and the insulating film by etching back the insulating film for the sidewall, after the step of performing anisotropic etching to the polycrystalline silicon film.

17. The manufacturing method of the semiconductor memory device according to claim 10, wherein

the tunnel insulating film has a thickness of 3 nm to 9 nm.

18. The manufacturing method of the semiconductor memory device according to claim 10, wherein

the Al_2O_3 film and the pair of charge storage layers have a thickness of 5 nm to 15 nm.

19. The manufacturing method of the semiconductor memory device according to claim 11, wherein

the tunnel insulating film has a thickness of 3 nm to 9 nm.

20. The manufacturing method of the semiconductor memory device according to claim 11, wherein

the Al_2O_3 film and a pair of charge storage layers have a thickness of 5 nm to 15 nm.